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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/837,734	04/17/2001	Takaaki Nagai	NECF 18.591	9062	
26304	7590 02/08/2005		EXAM	EXAMINER	
	MUCHIN ZAVIS ROSE	OWENS, DOUGLAS W			
	ON AVENUE C. NY 10022-2585		ART UNIT	PAPER NUMBER	
			2811		
			DATE MAILED: 02/08/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)			
Office Action Summany		09/837,734	NAGAI, TAKAAKI			
	Office Action Summary	Examiner	Art Unit			
		Douglas W. Owens	2811			
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
THE I - External after - If the - If NO - Failu Any	ORTENED STATUTORY PERIOD FOR REPLEMALING DATE OF THIS COMMUNICATION. Insions of time may be available under the provisions of 37 CFR 1. SIX (6) MONTHS from the mailing date of this communication. It period for reply specified above is less than thirty (30) days, a replement of the provisions of the	.136(a). In no event, however, may a reply be to ply within the statutory minimum of thirty (30) da d will apply and will expire SIX (6) MONTHS fror te, cause the application to become ABANDON	mely filed  ys will be considered timely.  n the mailing date of this communication.  ED (35 U.S.C. § 133).			
Status						
1)⊠	Responsive to communication(s) filed on <u>21 January 2005</u> .					
	his action is <b>FINAL</b> . 2b)⊠ This action is non-final.					
3)	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
	closed in accordance with the practice under	Ex parte Quayle, 1935 C.D. 11, 4	.53 O.G. 213.			
Dispositi	on of Claims					
4)⊠ Claim(s) <u>1,2 and 5-8</u> is/are pending in the application.						
	4a) Of the above claim(s) is/are withdrawn from consideration.					
5) Claim(s) is/are allowed.						
·	⊠ Claim(s) <u>1,2,5-8</u> is/are rejected.					
·	7) Claim(s) is/are objected to.					
. 8)∐	Claim(s) are subject to restriction and/	or election requirement.				
Applicati	on Papers					
9)[	The specification is objected to by the Examin	er.				
10) The drawing(s) filed on is/are: a) □ accepted or b) □ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority u	ınder 35 U.S.C. § 119					
a)[	Acknowledgment is made of a claim for foreig  All b) Some * c) None of:  1. Certified copies of the priority document according to the priority document application from the International Bureasee the attached detailed Office action for a list	nts have been received. Its have been received in Applica ority documents have been receiv au (PCT Rule 17.2(a)).	tion No red in this National Stage			
Attachmen	t(s)					
1) Notice of References Cited (PTO-892)  4) Interview Summary (PTO-413)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  Paper No(s)/Mail Date						
3) Infor	te of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO-1449 or PTO/SB/08 or No(s)/Mail Date		Patent Application (PTO-152)			

### **DETAILED ACTION**

#### Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 21, 2005 has been entered.

# Claim Rejections - 35 USC § 112

- 2. The following is a quotation of the first paragraph of 35 U.S.C. 112:
  - The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
- 3. Claims 1, 2 and 5-8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.
- Claims 1, 2, 7 and 8 require that the insulating layer formed directly below the floating gate and the gate of the select transistor form a tunneling gate oxide. There is no discussion in the specification or drawings, wherein the insulating layer directly below the select transistor forms a tunneling gate oxide. The specification discloses a final structure having a first insulating layer directly below the floating gate, which forms

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a tunneling oxide, and a second insulating layer directly below the select gate, which forms a gate insulator.

## Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 4,907,198 to Arima.

Arima teaches a non-volatile semiconductor storage apparatus (Figs. 10 A-10 I) comprising:

a memory cell array (Fig. 8) which has unit cells arranged in a rectangular matrix shape, said unit cell including:

a memory cell field effect transistor having a floating gate (2) and a control gate (28); and

a select field effect transistor having a diffused region (8) connected to a diffused region (8) of the memory cell field effect transistor, said floating gate and control gate extending to a position above a gate (3) of said select field effect transistor, top and bottom surfaces of the floating gate control gate being parallel to top and bottom surfaces of the select field effect transistor, an insulating layer (21,6;) formed directly below the floating gate and the select gate, wherein the portion under the floating gate is used as a tunneling gate oxide in a region to be an active region of the unit cell.

Arima teaches that the diffusion layer (8) is used as a source for the select transistor and the field effect transistor, as opposed to being a drain for the select transistor and source for the memory cell field effect transistor. However, this is a suggested use limitation, since the source/drain is a matter of how and where potential is applied. Accordingly, the requirement of the region being used as a drain for the select transistor connected to a source of the memory field effect transistor is not given any patentable weight, since it does not distinguish the structure of the claimed invention from that of the prior art.

## Response to Arguments

6. Applicant's arguments filed November 23, 2004 have been fully considered but they are not persuasive.

Applicant argues that Arima does not teach an EEPROM, wherein a tunnel oxide is in a region to be an active region of the unit cell. This teaching can be seen in Fig. 10 I, where the tunnel oxide (6) is in an active region.

#### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Douglas W Owens

Dougla W. Owen

Examiner Art Unit 2811